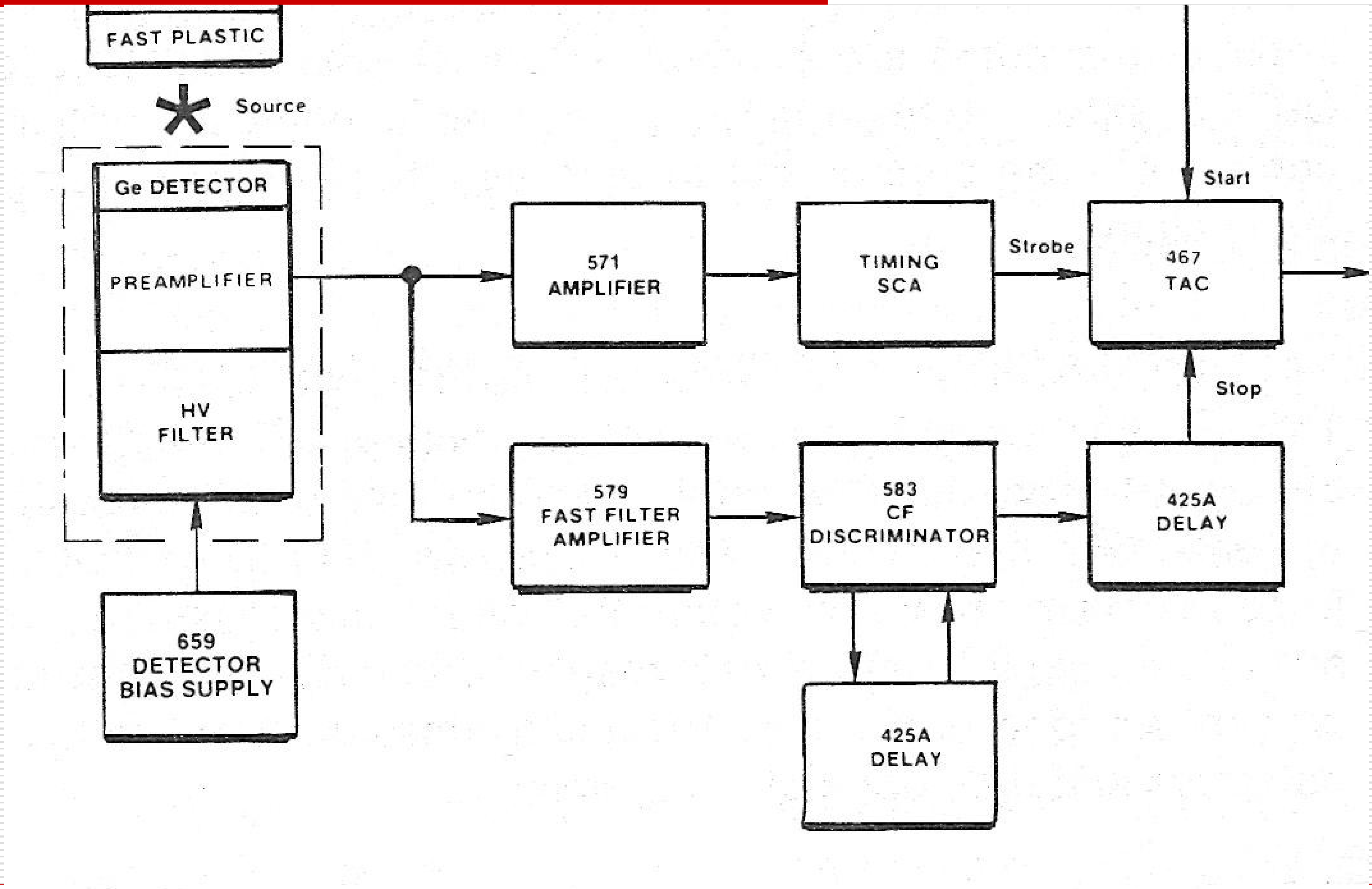
Digital Pulse Processing: A new paradigm in nuclear instrumentation

Roberto V. Ribas – DFN-IFUSP

Nuclear Instrumentation Modules - NIM



Spectroscopic Amplifier

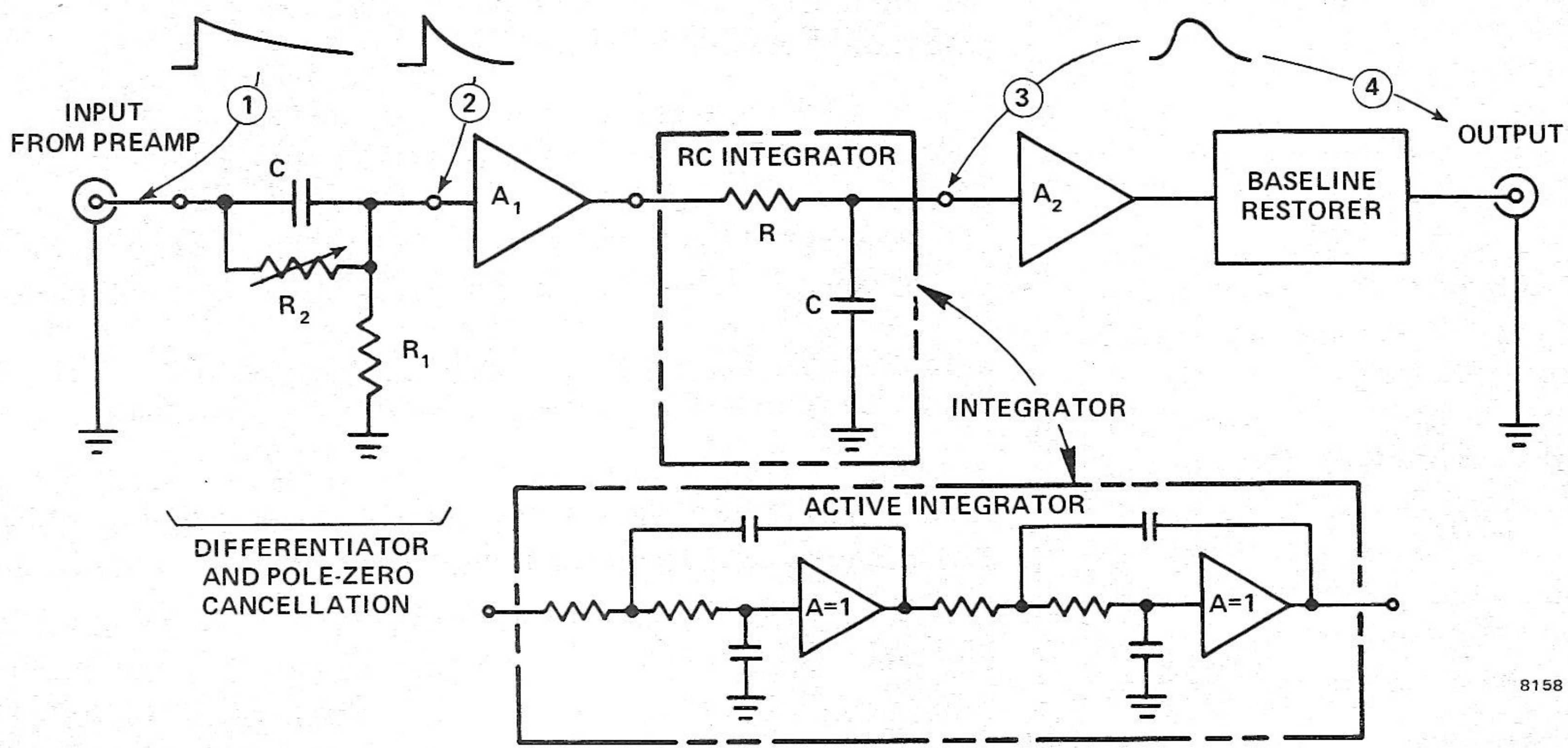
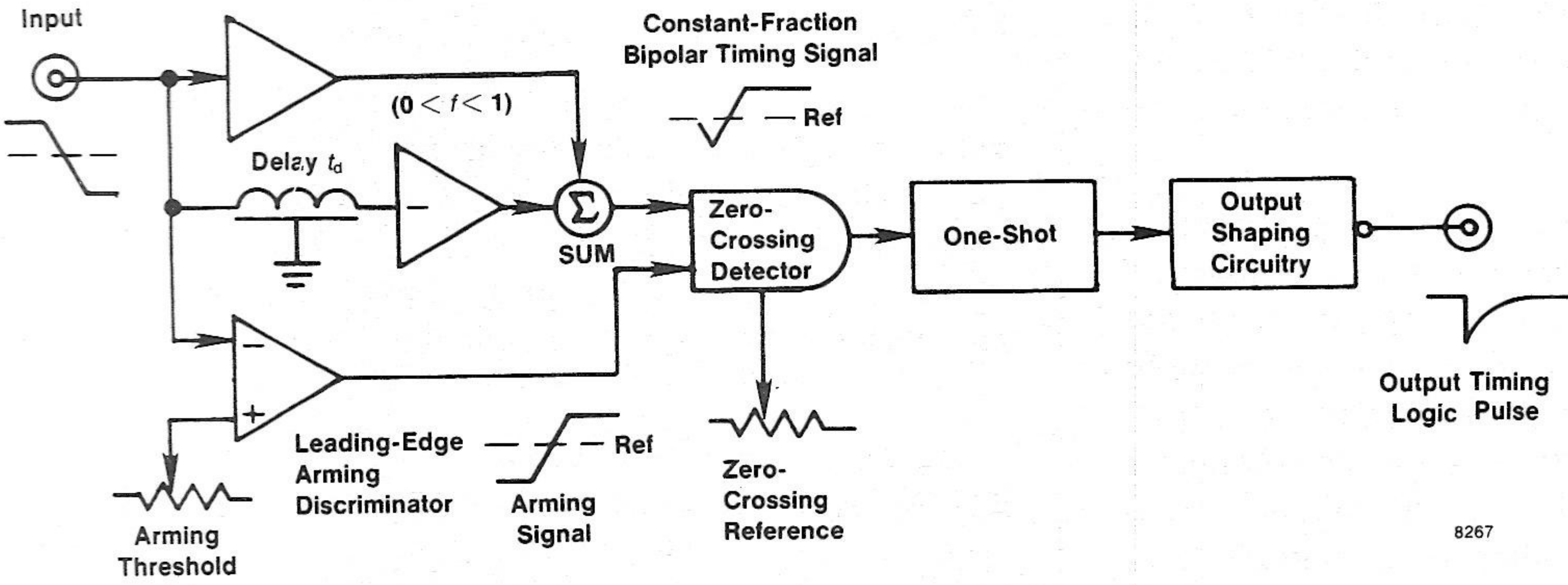
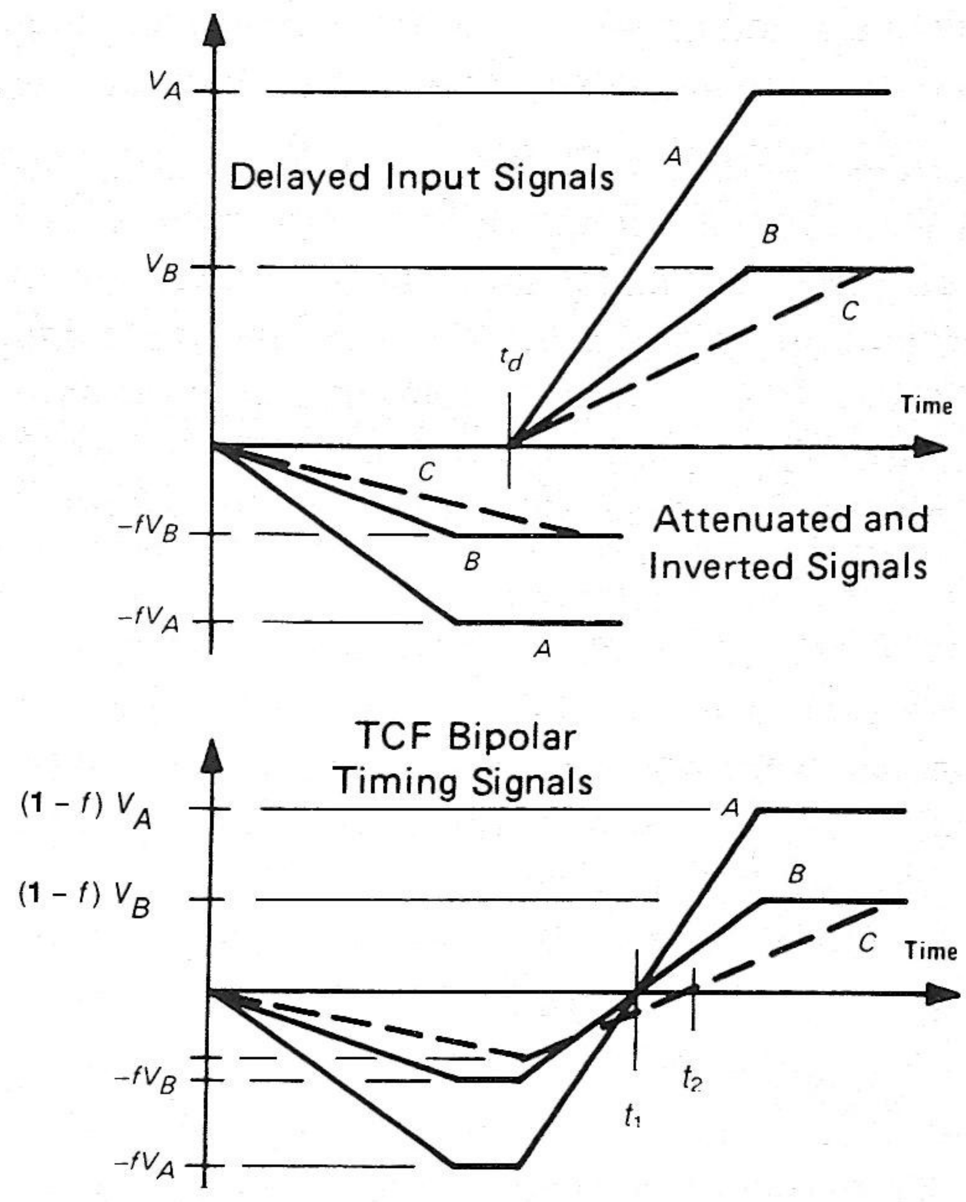


Fig. 11. Pulse Shaping in the Semi-Gaussian Shaping Amplifier.

Constant Fraction Discriminator



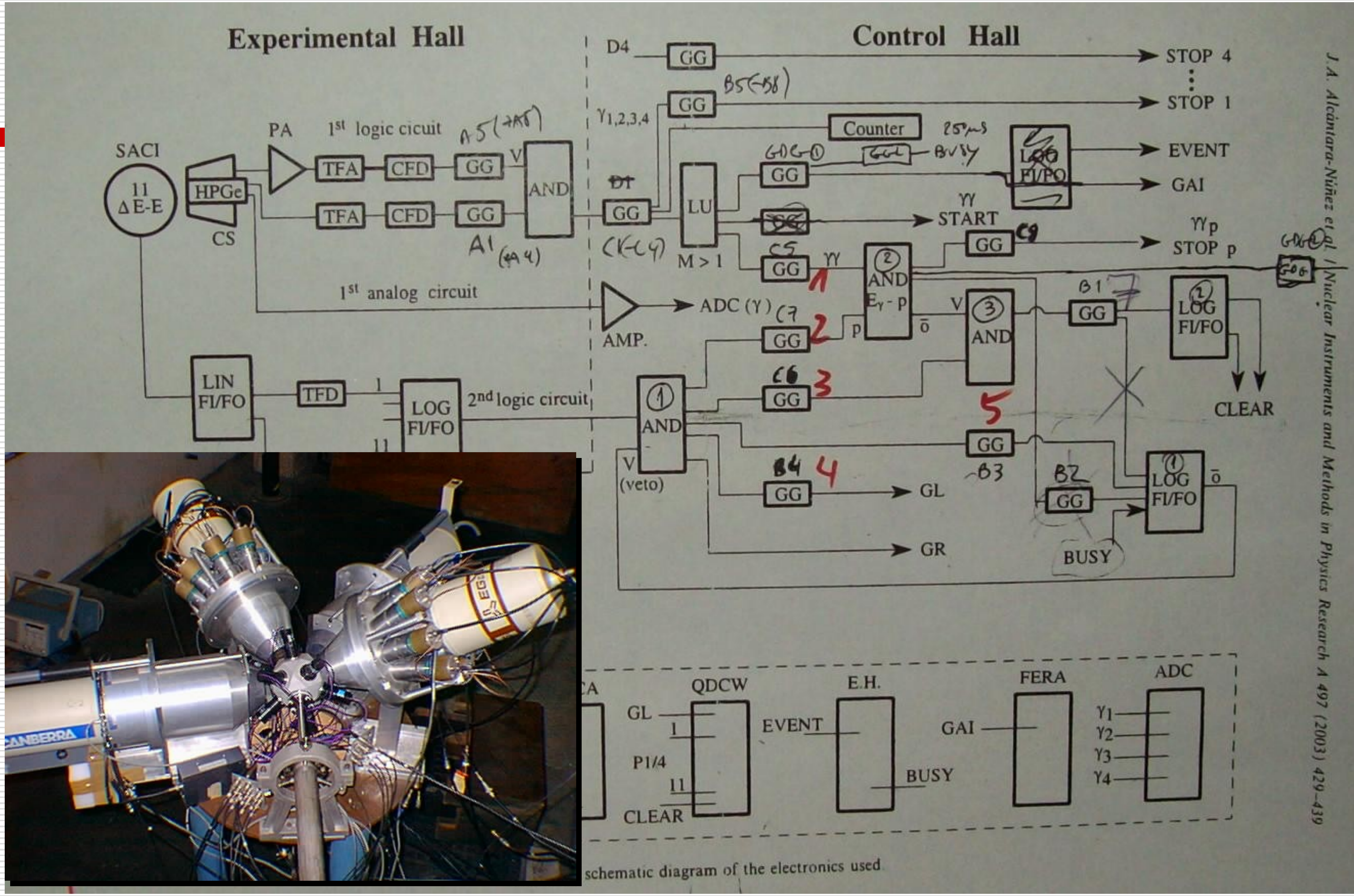
CFD



V_A
Delayed Input Signals
A
V_B
B
C
t_d
Time
C
Attenuated and
Inverted Signals
$-fV_B$
B
$-fV_A$
A
TCF Bipolar
Timing Signals
$(1-f)\ V_A$
A
$(1-f)\ V_B$
B
C
Time
$-fV_B$
t_2
t_1
$-fV_A$

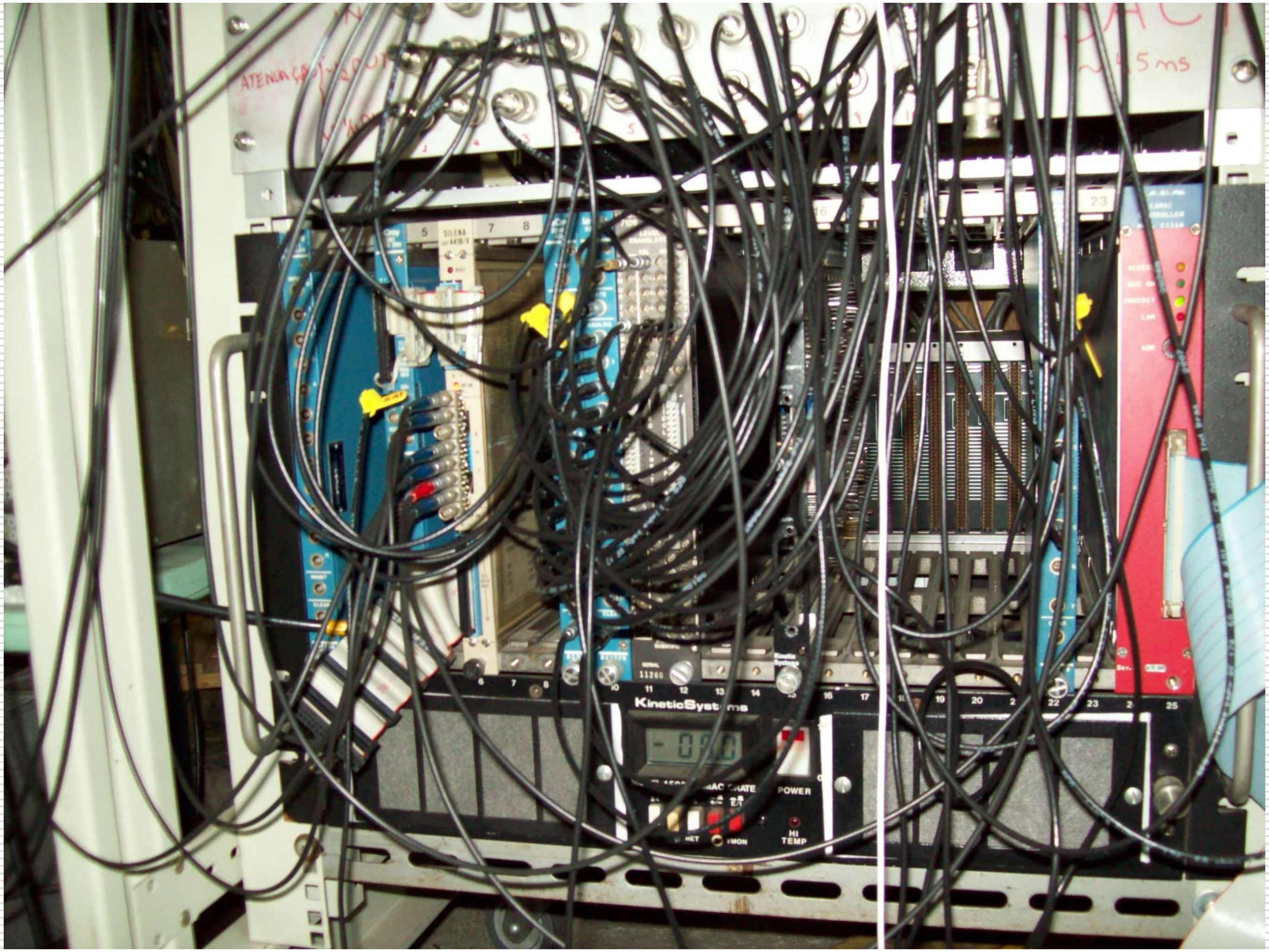
Multichannel Analyzer (1970)

Saci-Pererê

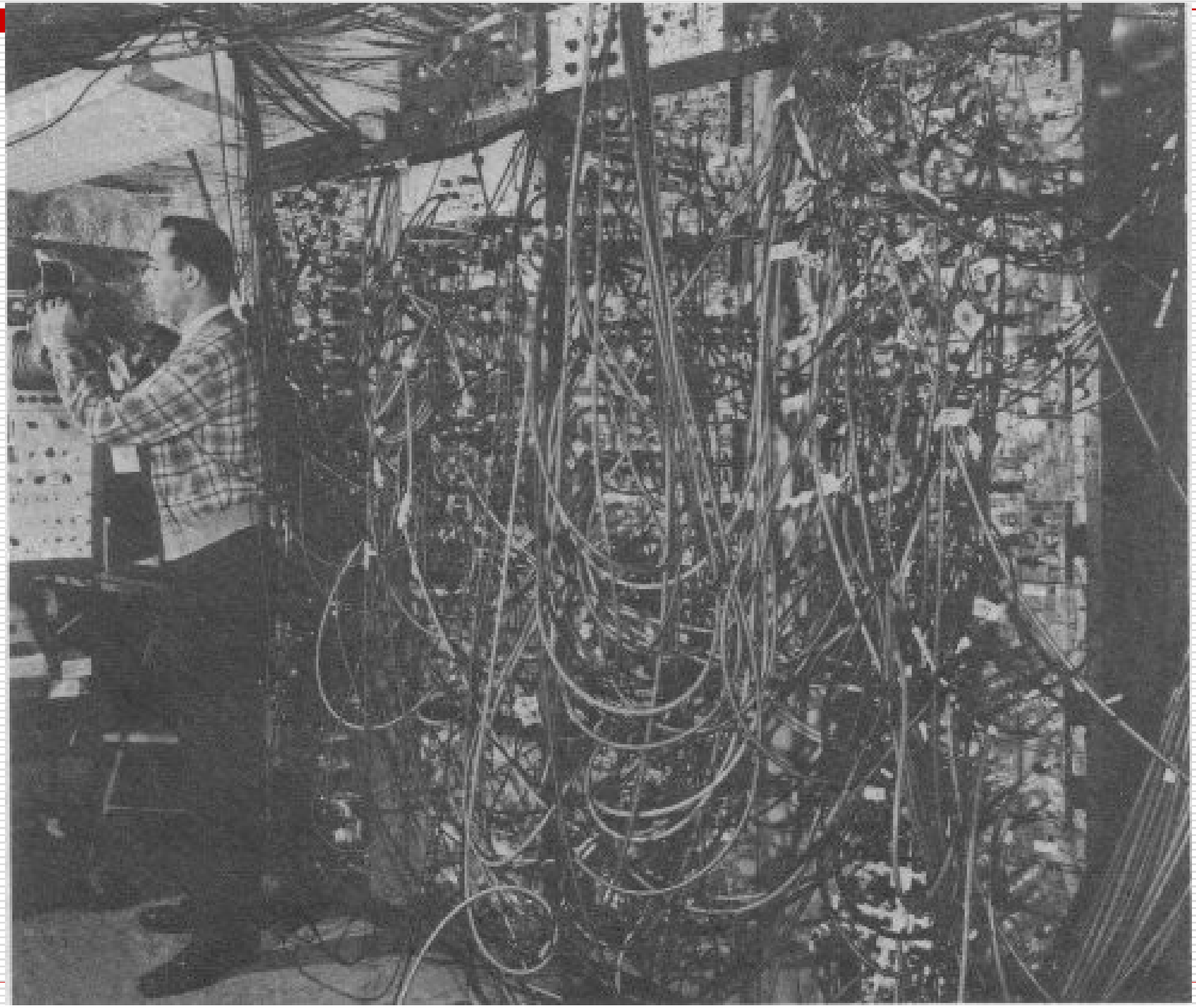


Experimental Hall
Control Hall
SACI
11
ΔE-E
HPGe
CS
PA
1st logic cicuit
TFA
CFD
GG
AND
V
1st analog circuit
AMP.
ADC (γ)
LIN
FI/FO
TFD
LOG
FI/FO
2nd logic circuit
V
(veto)
D4
γ1,2,3,4
LU
M > 1
Counter
STOP 4
STOP 1
EVENT
GAI
START
STOP p
AND
Eγ - p
p
ō
CLEAR
GL
GR
BUSY
QDCW
E.H.
FERA
ADC
P1/4
γ1
γ2
γ3
γ4
schematic diagram of the electronics used
J.A. Alcántara-Núñez et al. / Nuclear Instruments and Methods in Physics Research A 497 (2003) 429–439

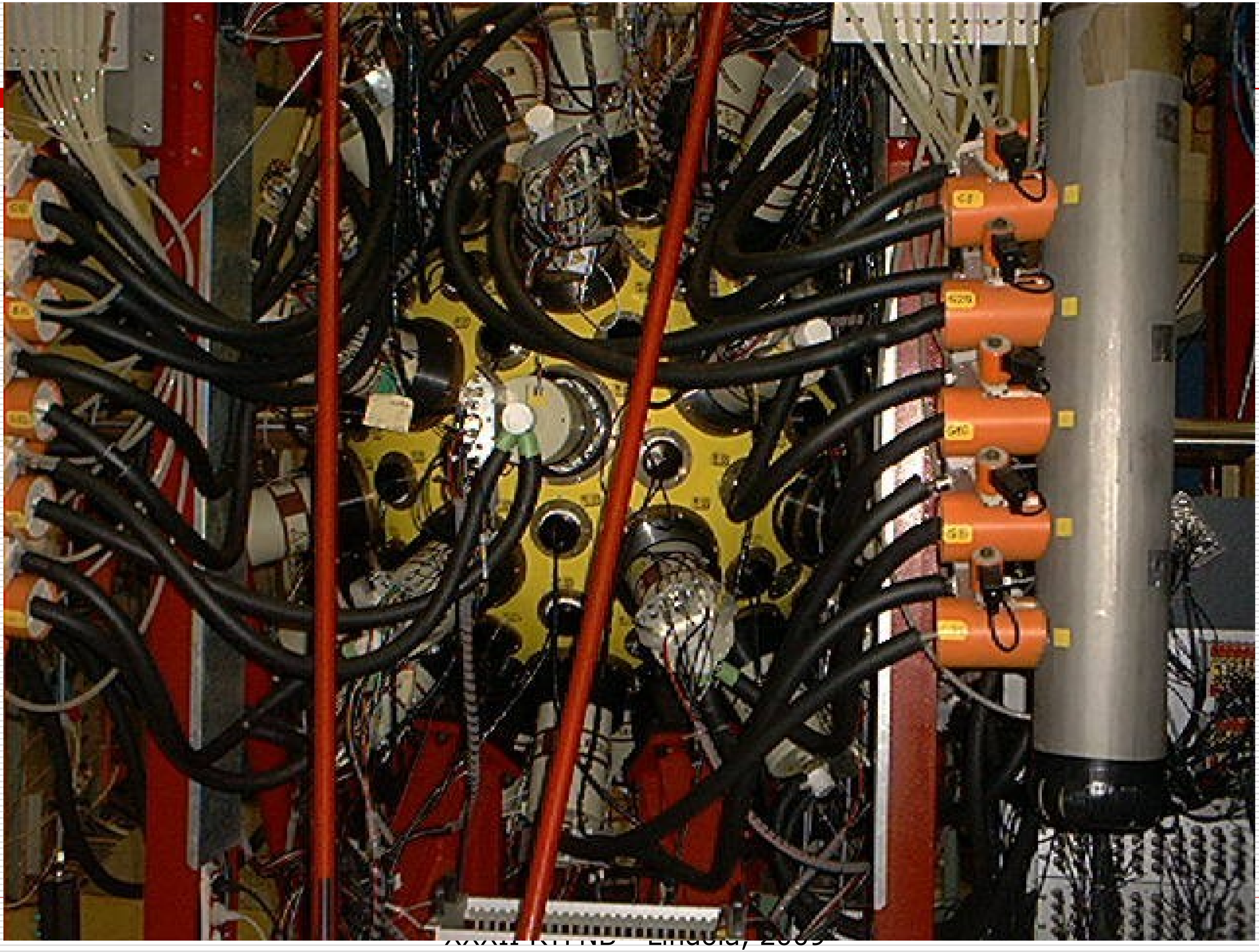
CAMAC - 1970



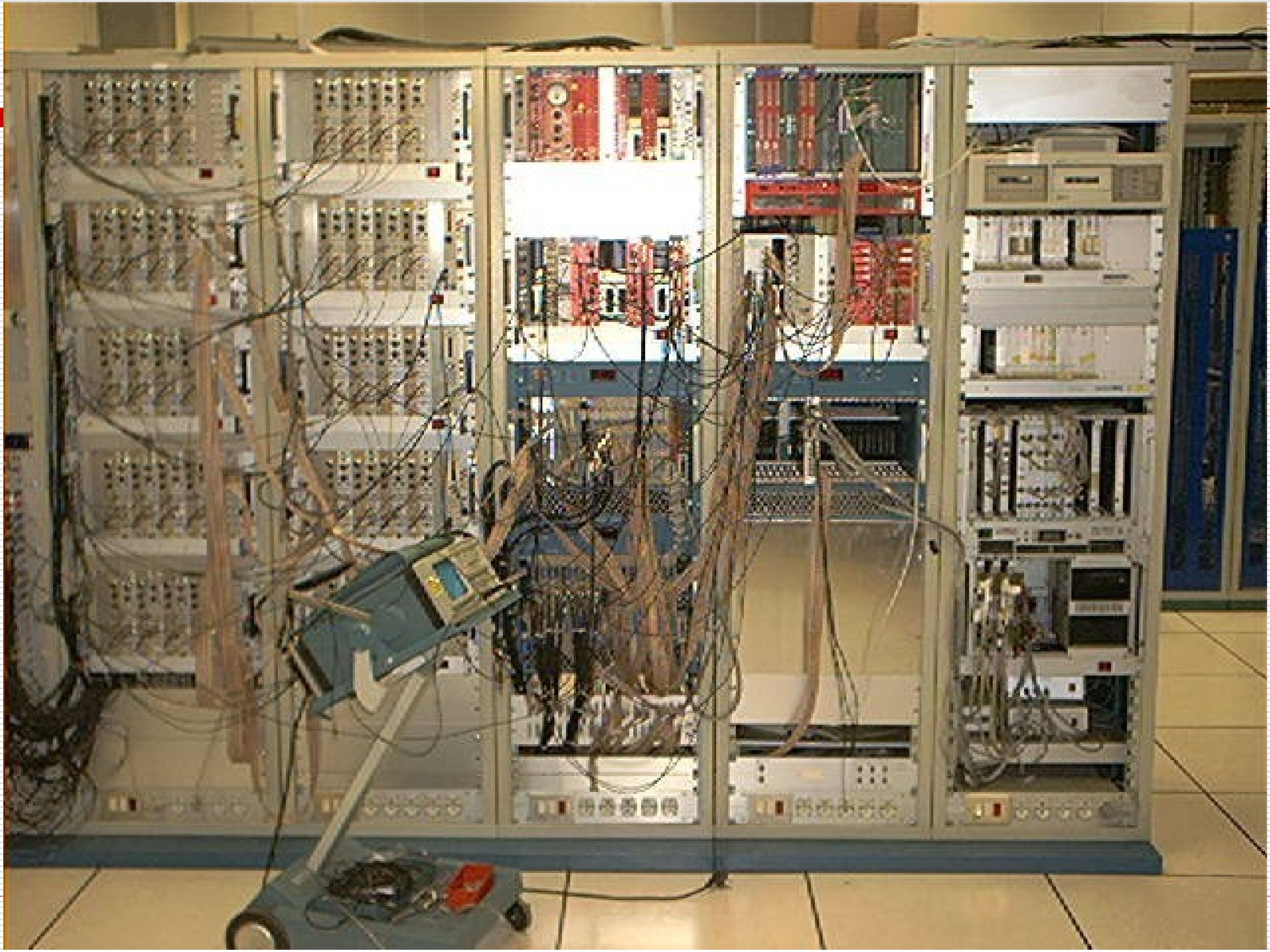
1960´s – Complexity of traditional systems comes to its limits...



GASP – 1990



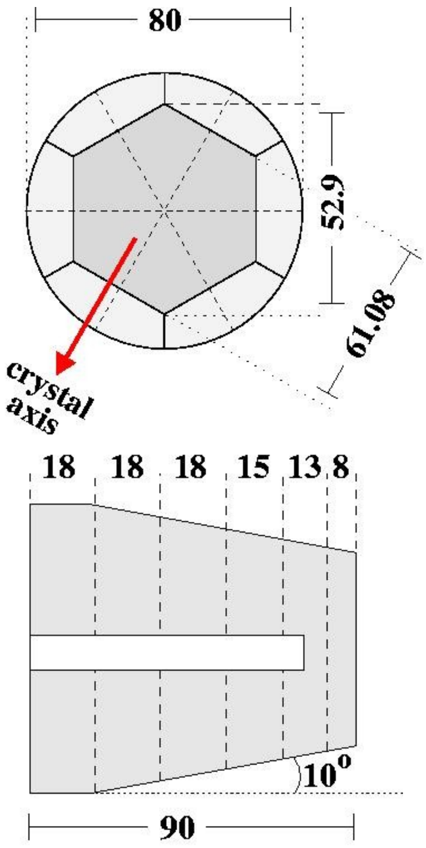
CAMAC + FERA + ...

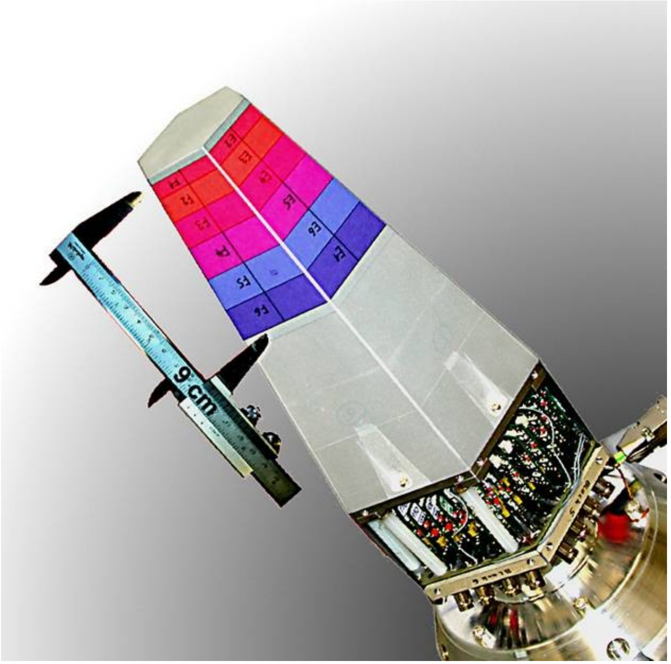


AGATA Prototypes *(Calin Ur - Guarujá, 2005)*

(Berta Rubio´s talk)

Symmetric detectors
- 3 ordered, Italy, Germany
- 3 delivered
- Acceptance tests in Koln
- 3 work very well





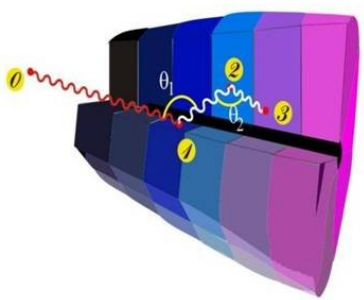
Encapsulation
0.8 mm Al walls
0.4 mm spacing

MINIBALL-style cryostat
used for acceptance tests
"standard" preamplifiers

Ingredients of Gamma-Ray Tracking (C. Ur)

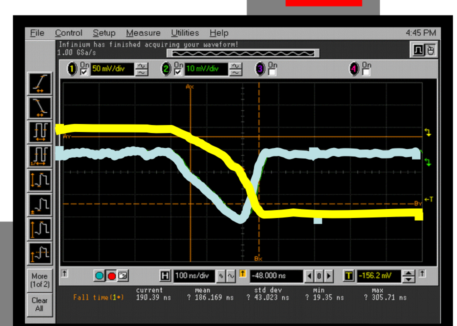
1

Highly segmented HPGe detectors



2

Digital electronics to record and process segment signals



3

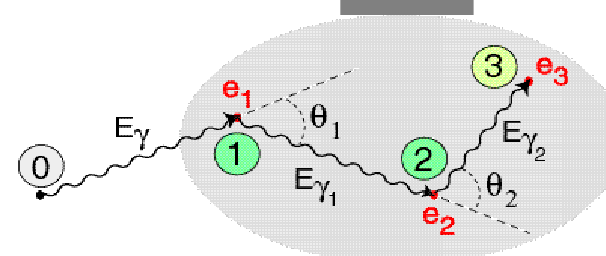
Pulse Shape Analysis to decompose recorded waves

Identified interaction points

$(x,y,z,E,t)_i$

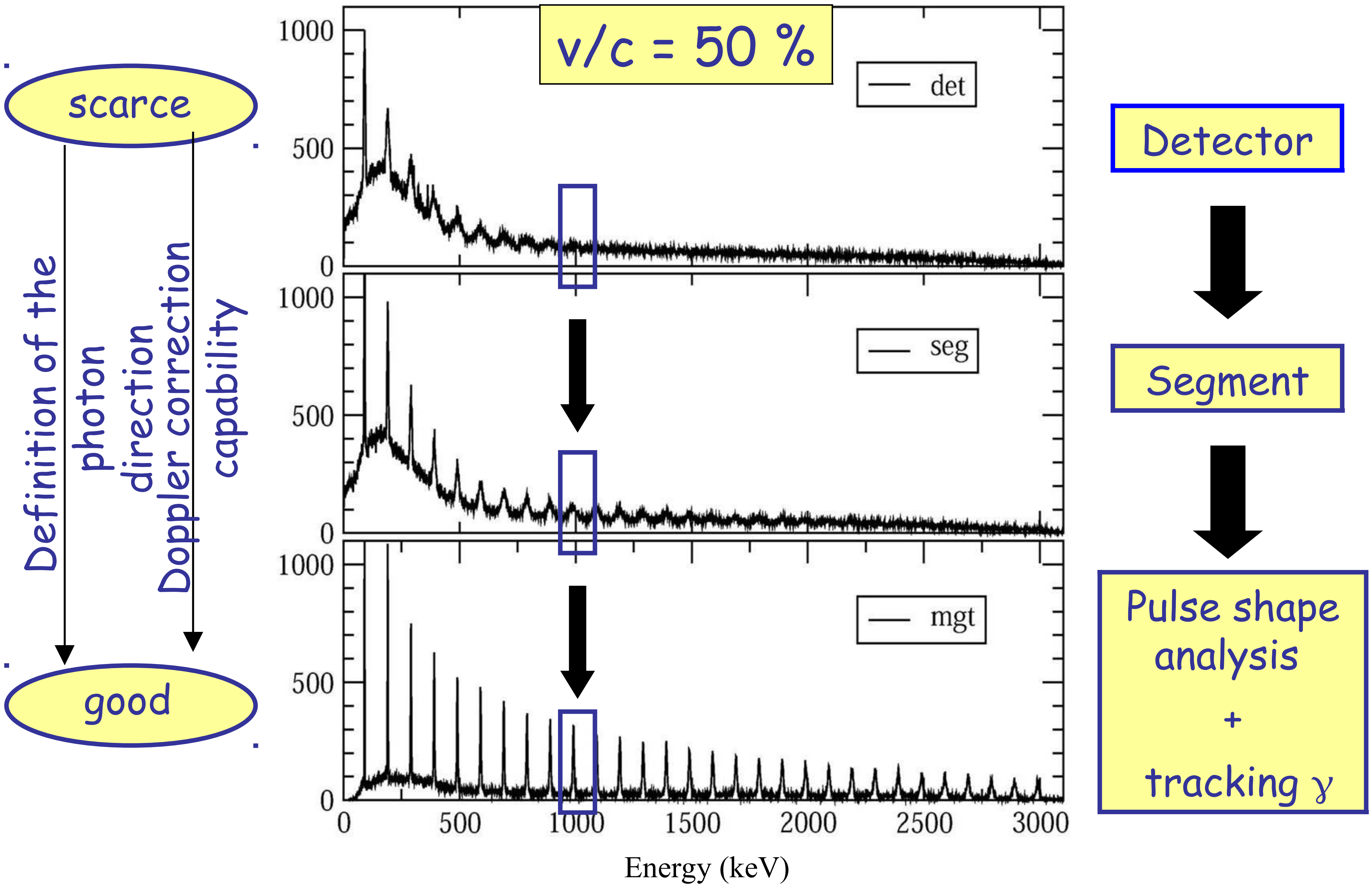
4

Reconstruction of tracks evaluating permutations of interaction points



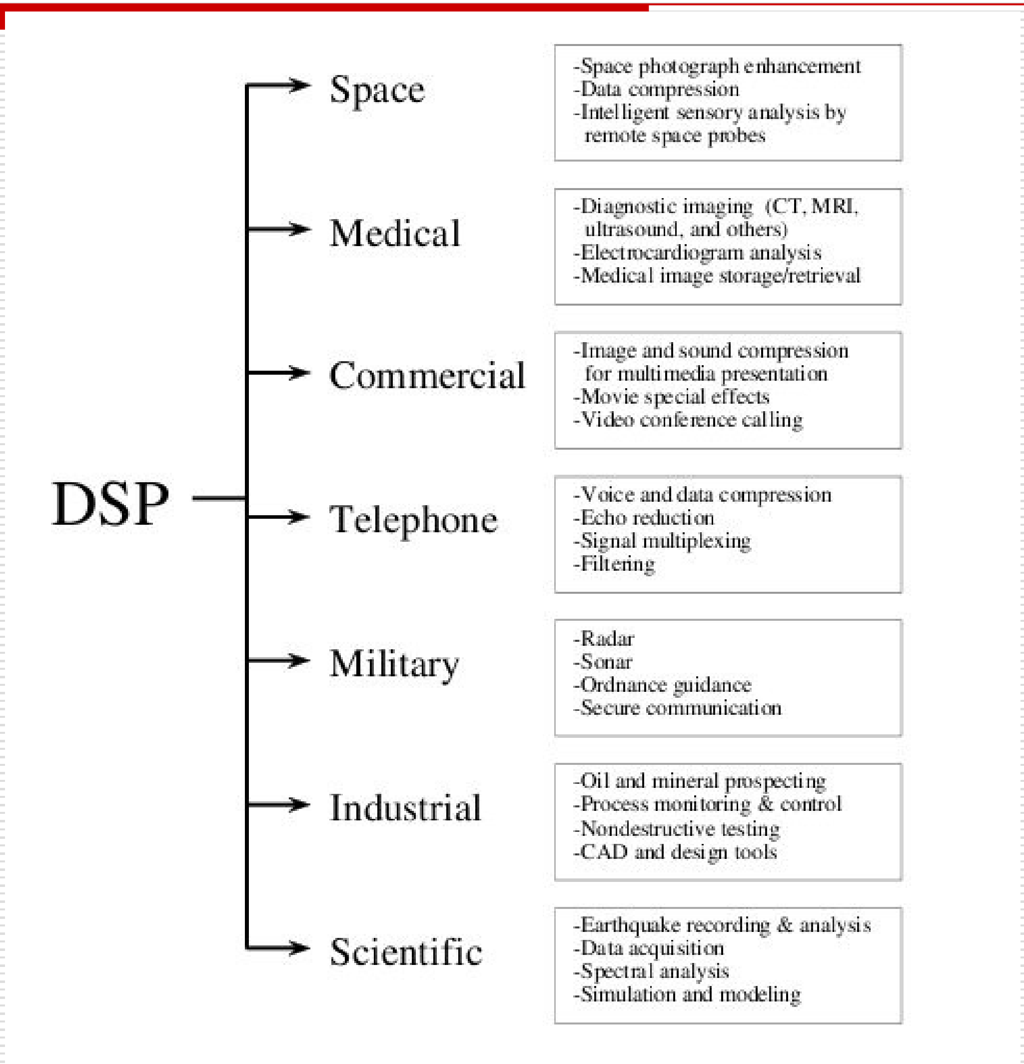
Reconstructed gamma-rays

Benefits of the γ-ray tracking (C. Ur)

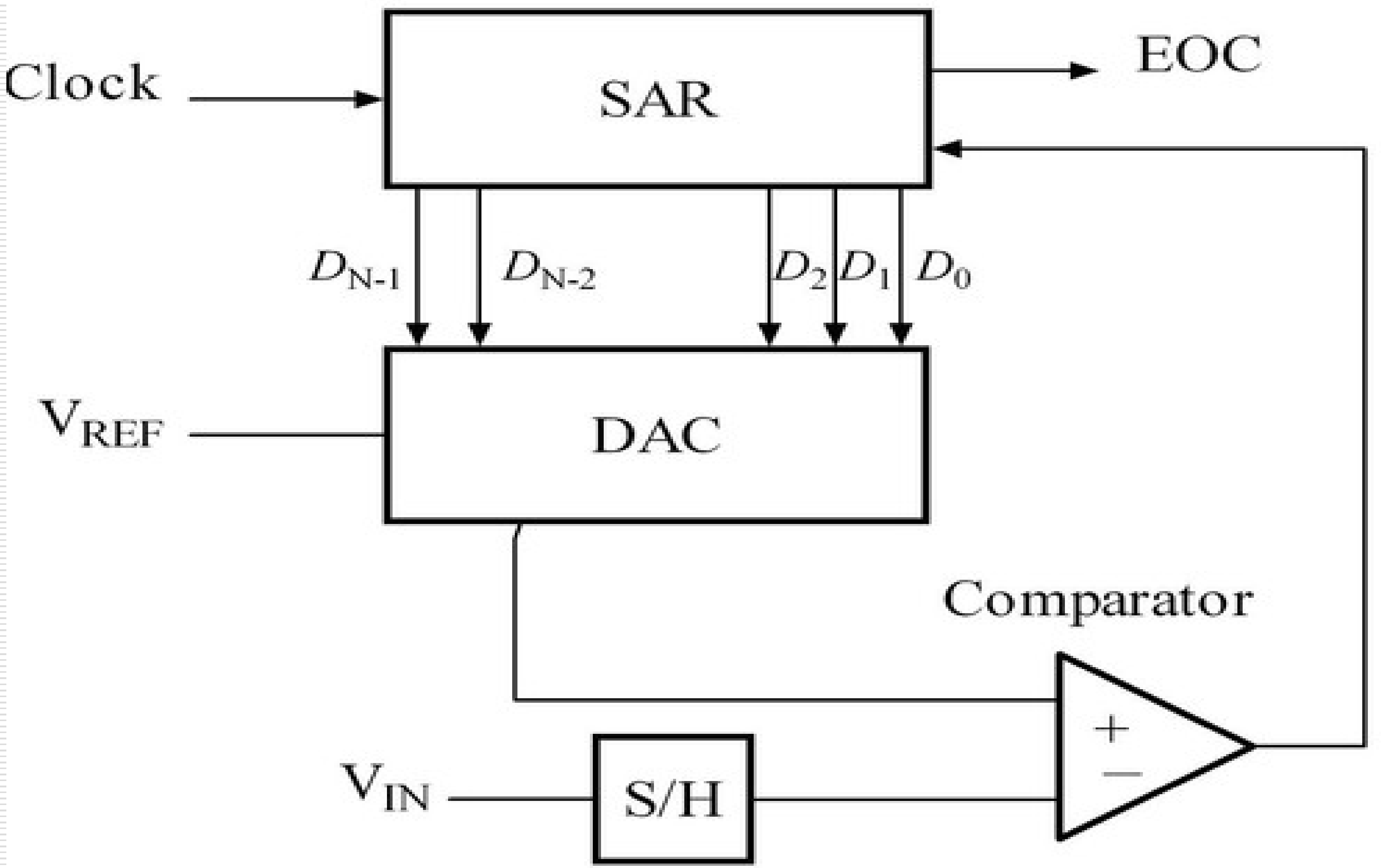


Data simulation by E.Farnea and F.Recchia (INFN Padova)

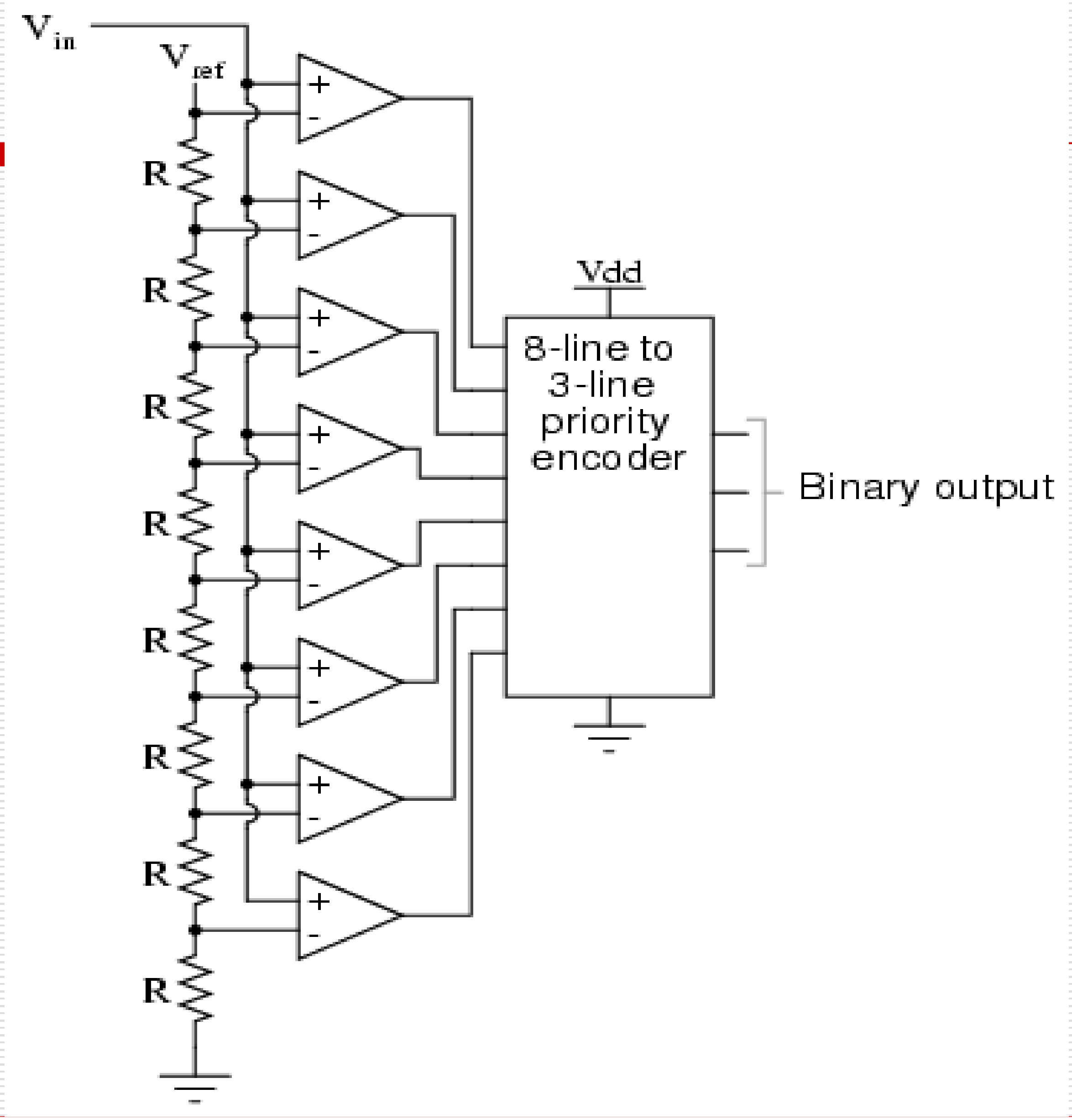
DIGITAL SIGNAL PROCESSING



SUCCESSIVE APPROXIMATION ADC

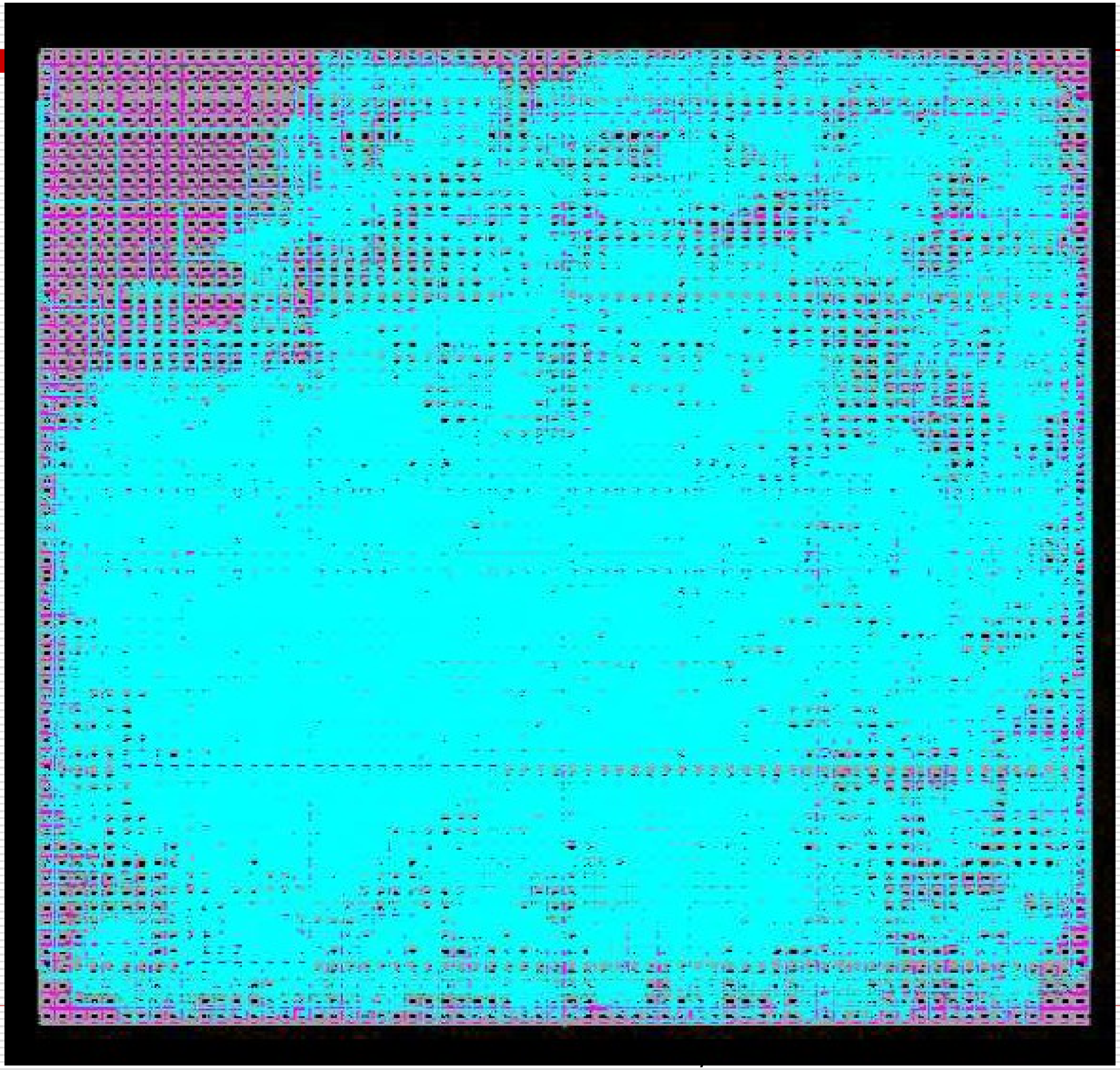


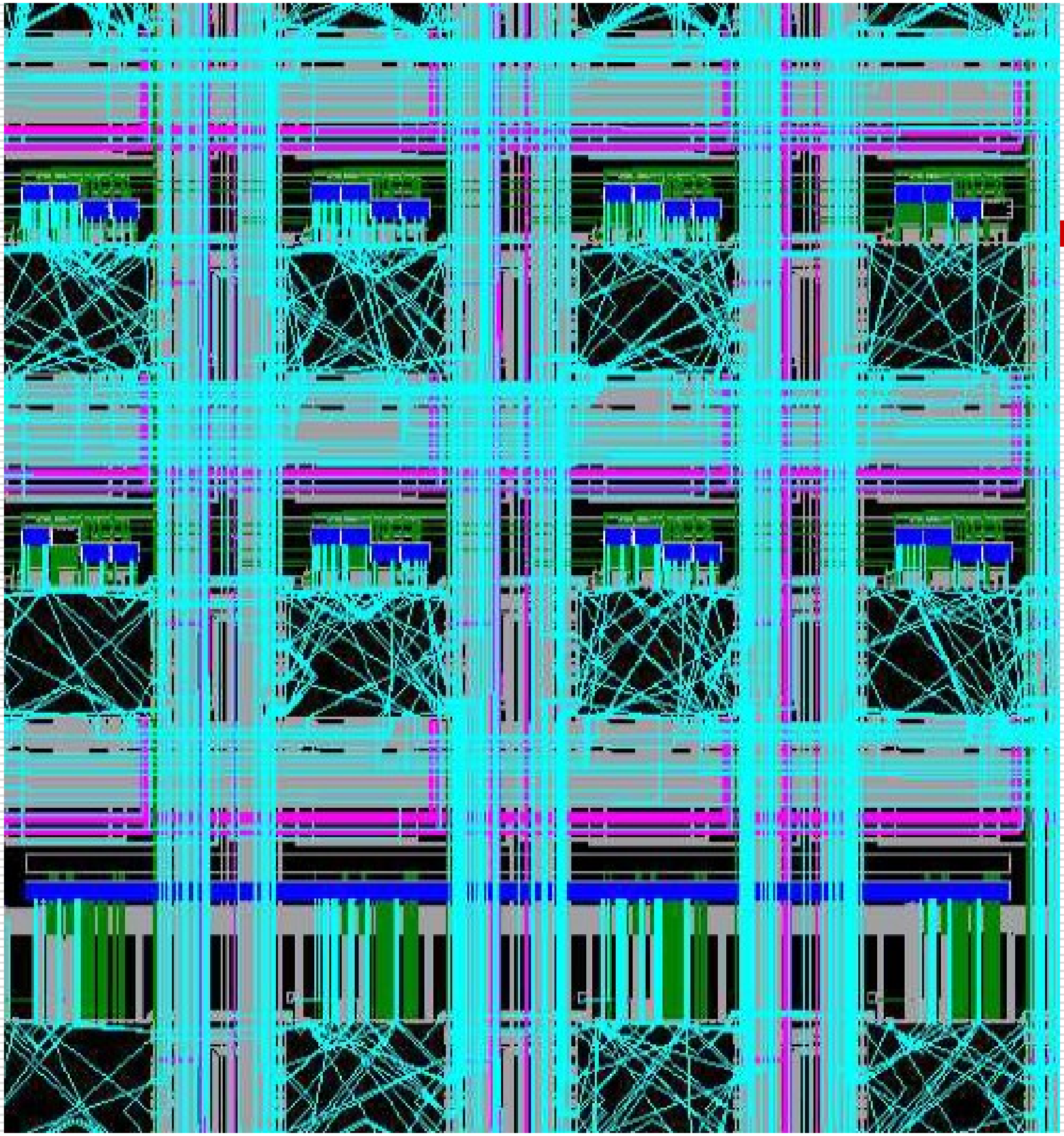
FLASH ADC

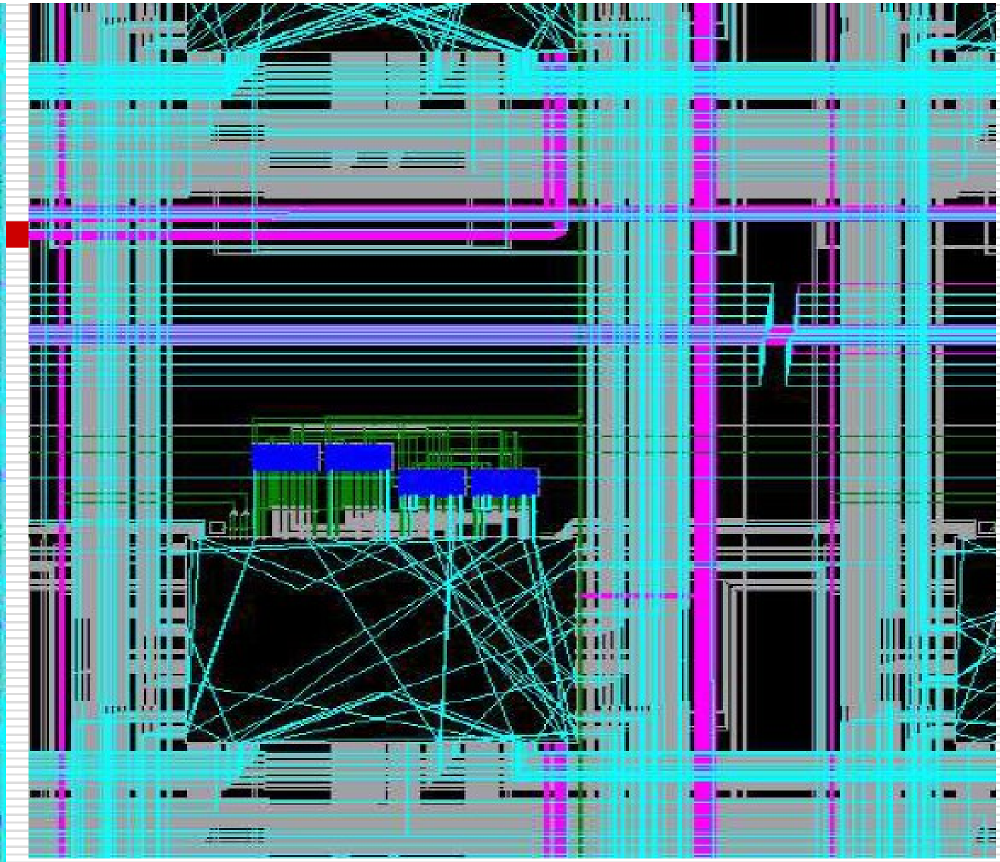


V in
V ref
R
R
R
R
R
R
R
R
Vdd
8-line to 3-line priority encoder
Binary output

FPGA - Field Programmable Gate Array (I.Y. Lee)







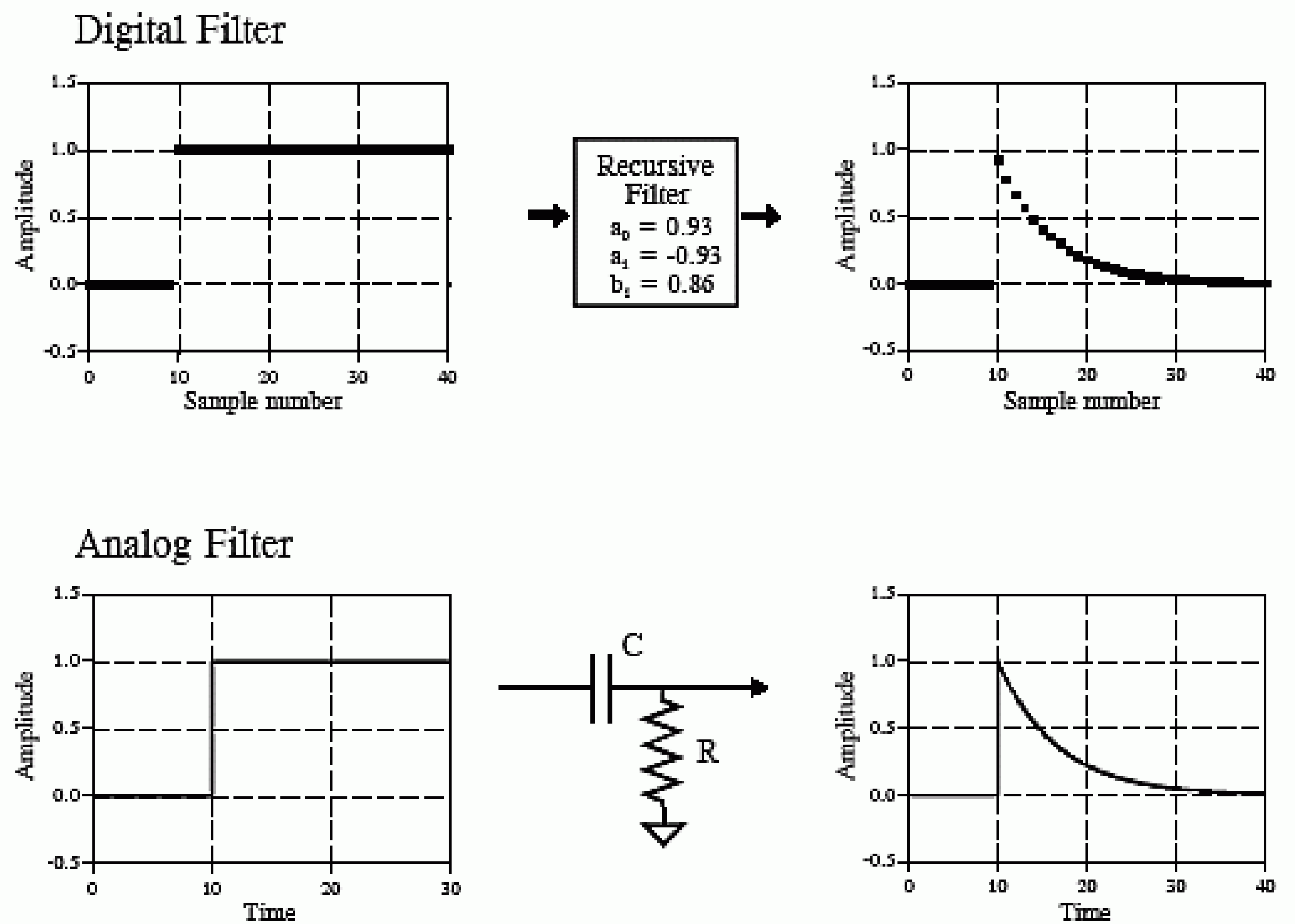


FIGURE 19-3
Single pole high-pass filter. Proper coefficient selection can also make the recursive filter mimic an electronic RC high-pass filter. These single pole recursive filters can be used in DSP just as you would use RC circuits in analog electronics.

(www.dspguide.com/)

$$y(i) = a_o*x(i)+a_1*x(i-1)+a_2*x(i-2)+b_1*y(i-1)+b_2*y(i-2)$$

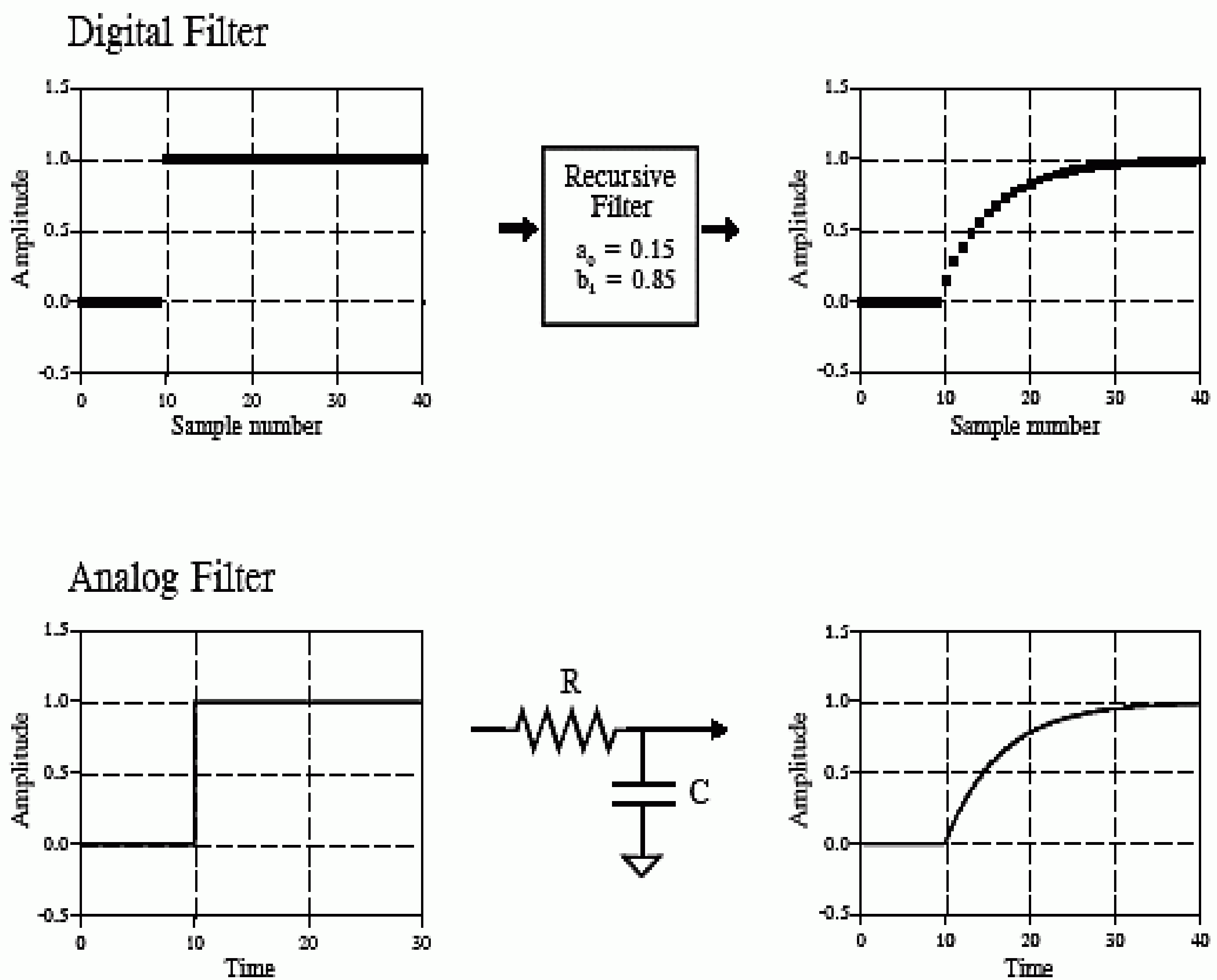


FIGURE 19-2
Single pole low-pass filter. Digital recursive filters can mimic analog filters composed of resistors and capacitors. As shown in this example, a single pole low-pass recursive filter smoothes the edge of a step input, just as an electronic RC filter.

Spectroscopic Amplifier

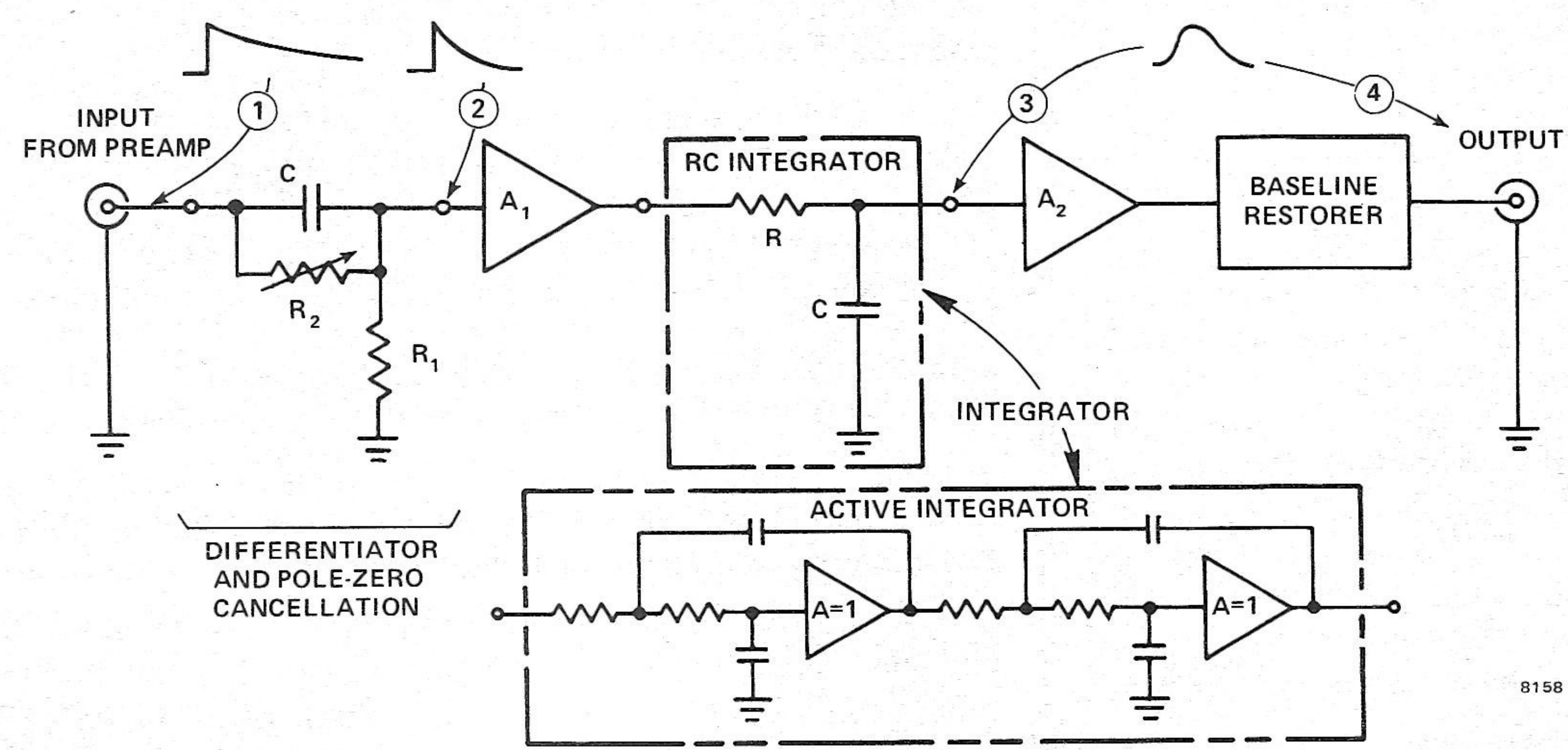


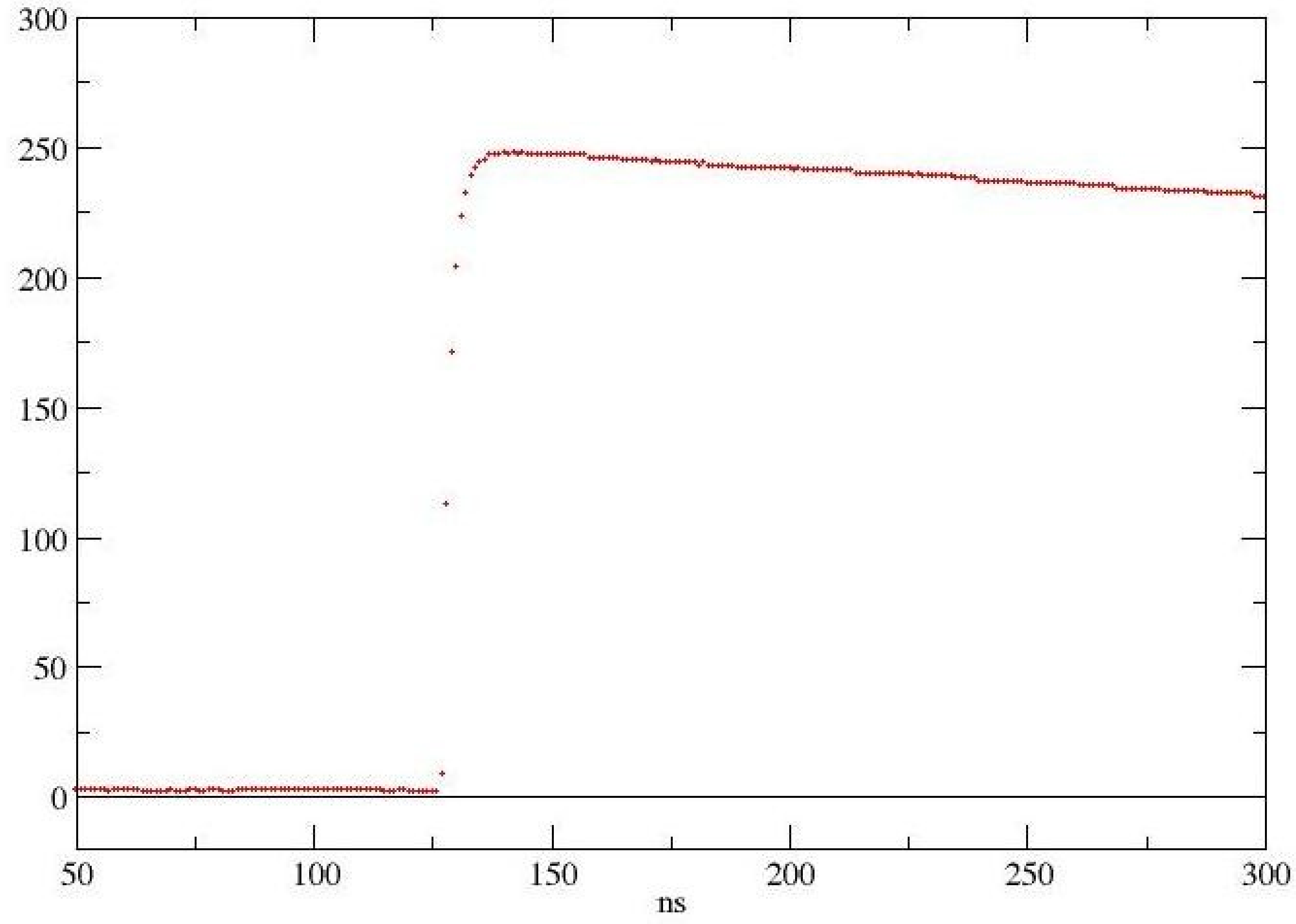
Fig. 11. Pulse Shaping in the Semi-Gaussian Shaping Amplifier.

DPP for typical NIM modules functions

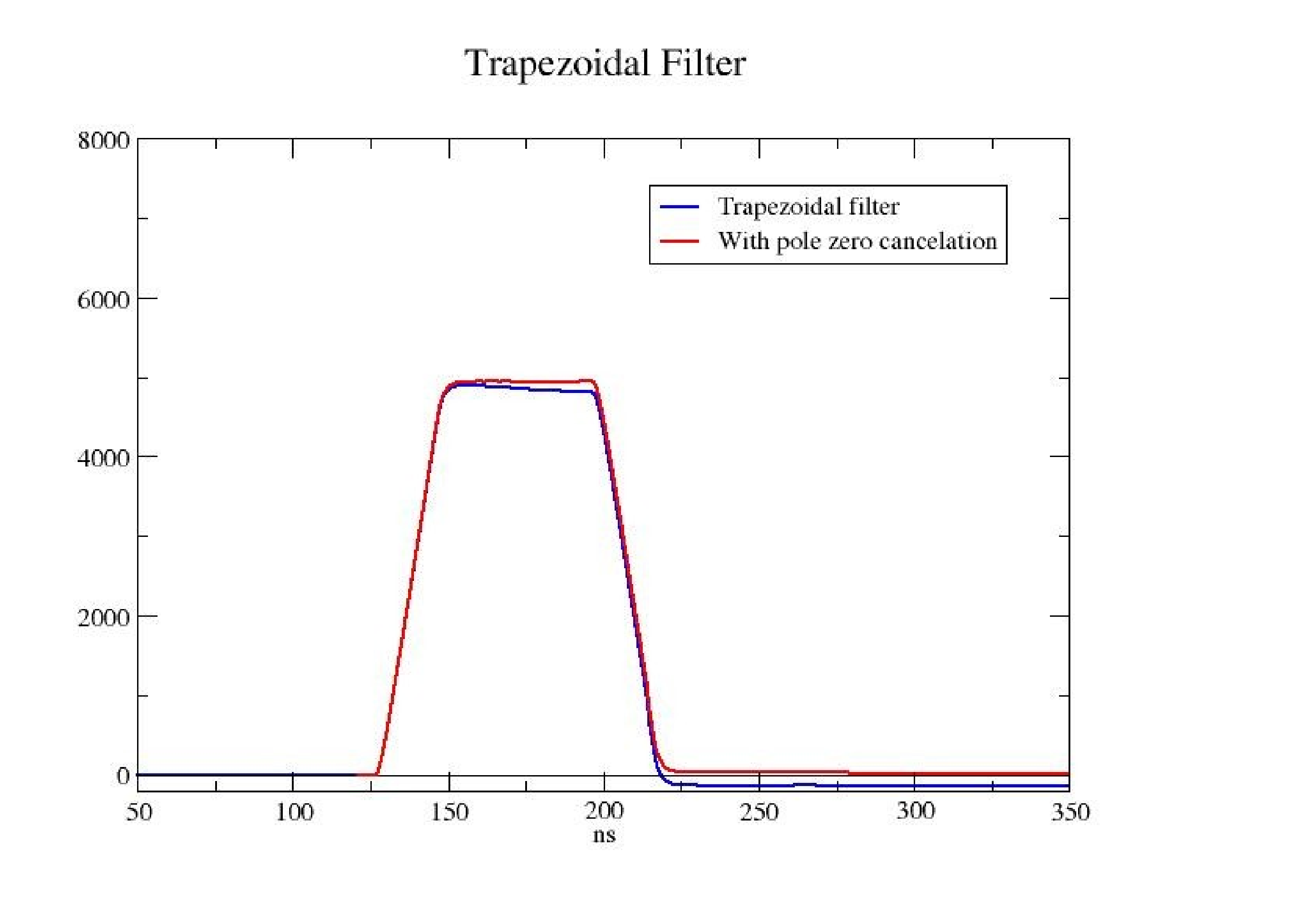
- *Leading Edge Discrimination:*
- •$y[n]=x[n]-x[n-k]$(*differentiation*)
- •$y[n]= (x[n]+x[n-2]) +x[n-1]<<1$(*Gaussian filtering*)
- •Threshold comparison →LED time
- *Constant Fraction Discrimination*:
- •$y[n]=x[n]-x[n-k]$(*differentiation*)
- •$y[n]= (x[n]+x[n-2]) +x[n-1]<<1$(*Gaussian filtering*)
- •$y[n]=x[n-k]<<a-x[n]$(*constant fraction*)
- •*Zero crossing comparison →CFD time*
- *Trapezoidal filter and energy determination*:
- •$y[n]=y[n-1]+ ((x[n]+x[n-2m-k]))–(x[n-m]+x[n-m-k]))$

J.T. Anderson et al. IEEE N25, 6 p1751 (2007)

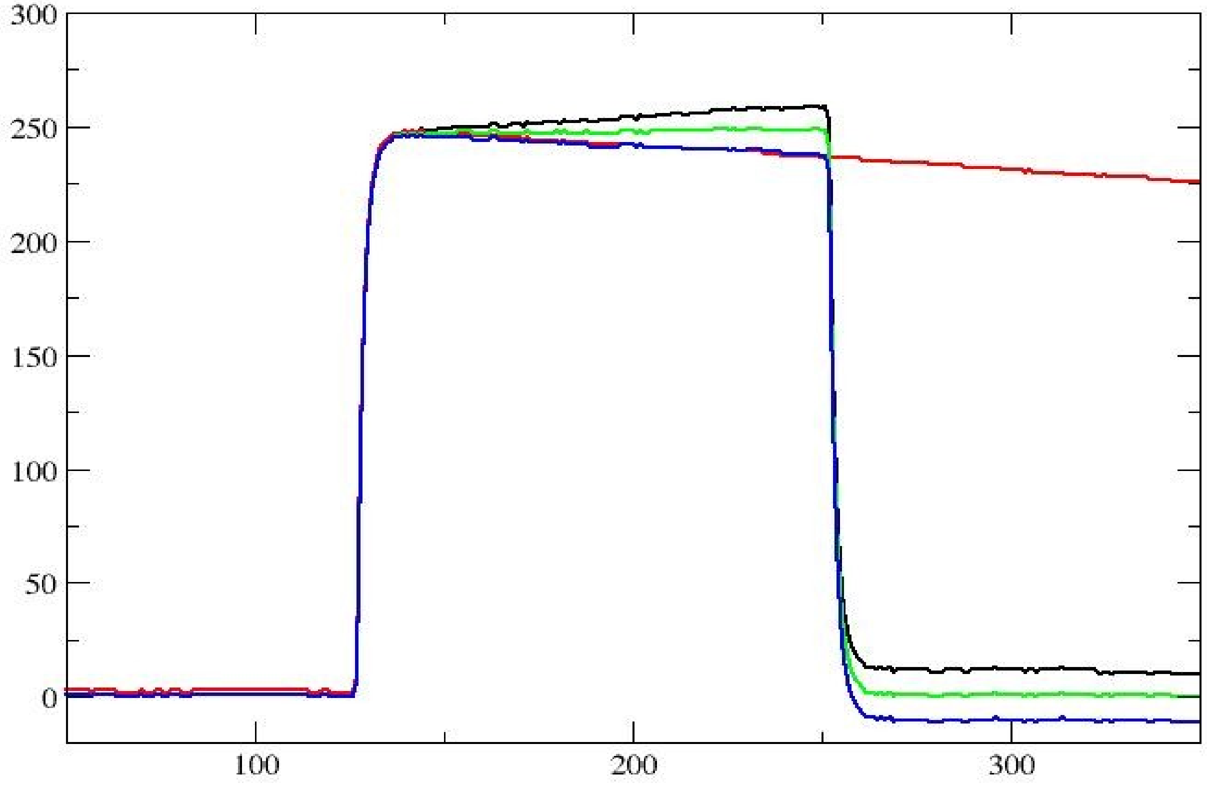
Pre-amp pulse



Trapezoidal Filter



Moving Window Deconvolution



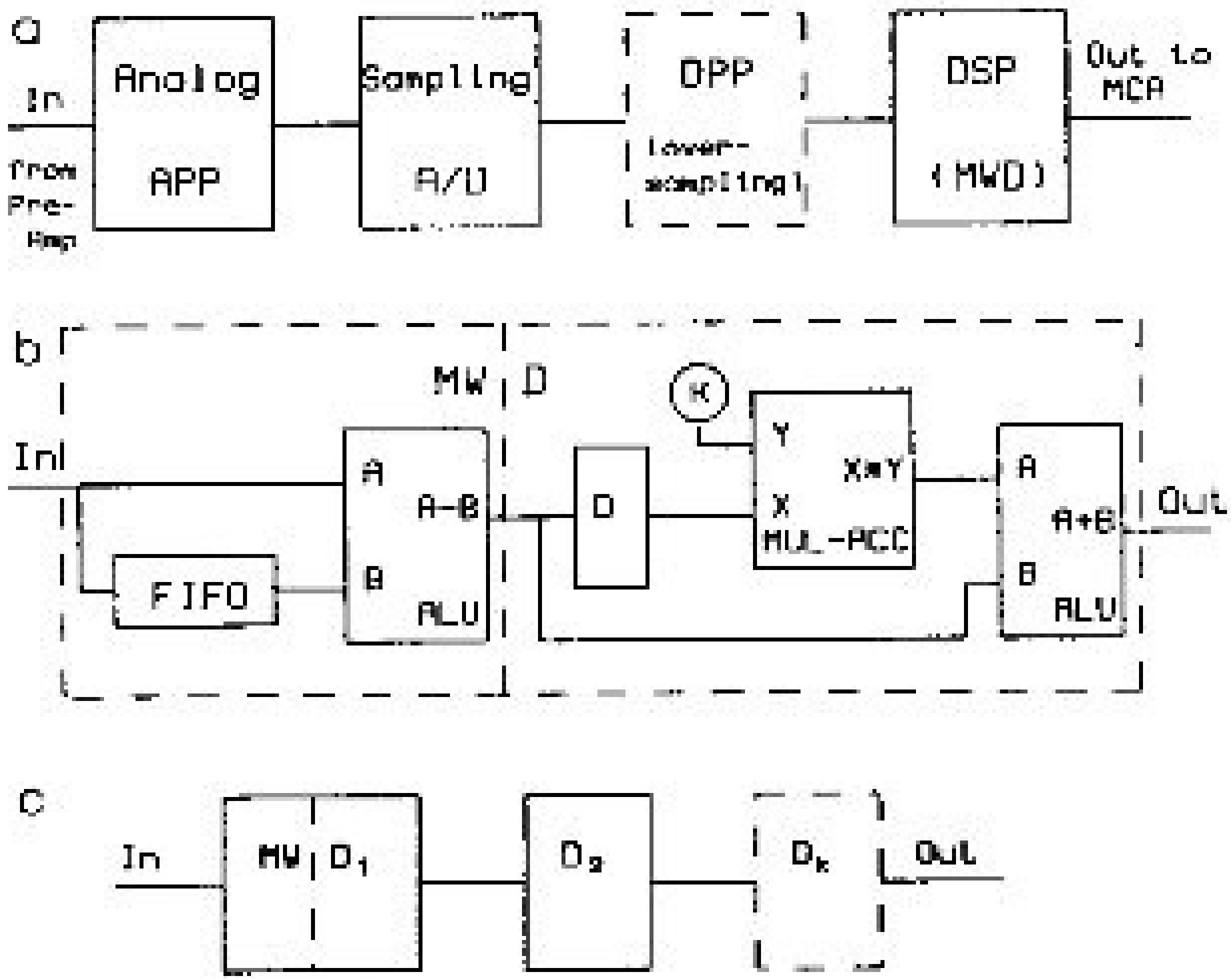
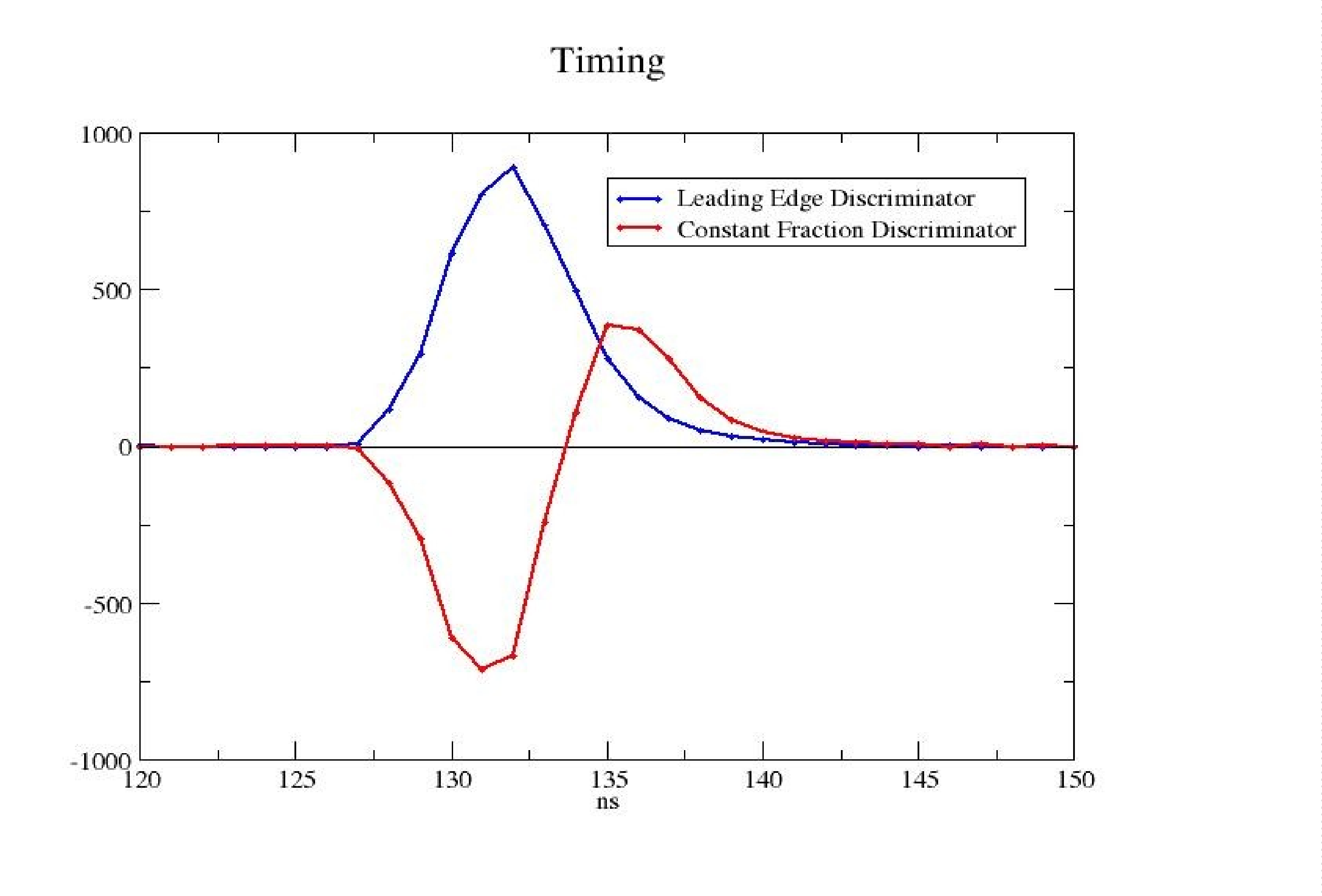


Figure 3: MWD-ADC block diagram (a), MWD process diagram (b) and cascade of moving deconvolvers (c).

Georgiev&Gast IEEE N40,4 p770 (1993)

Constant Fraction Discriminator

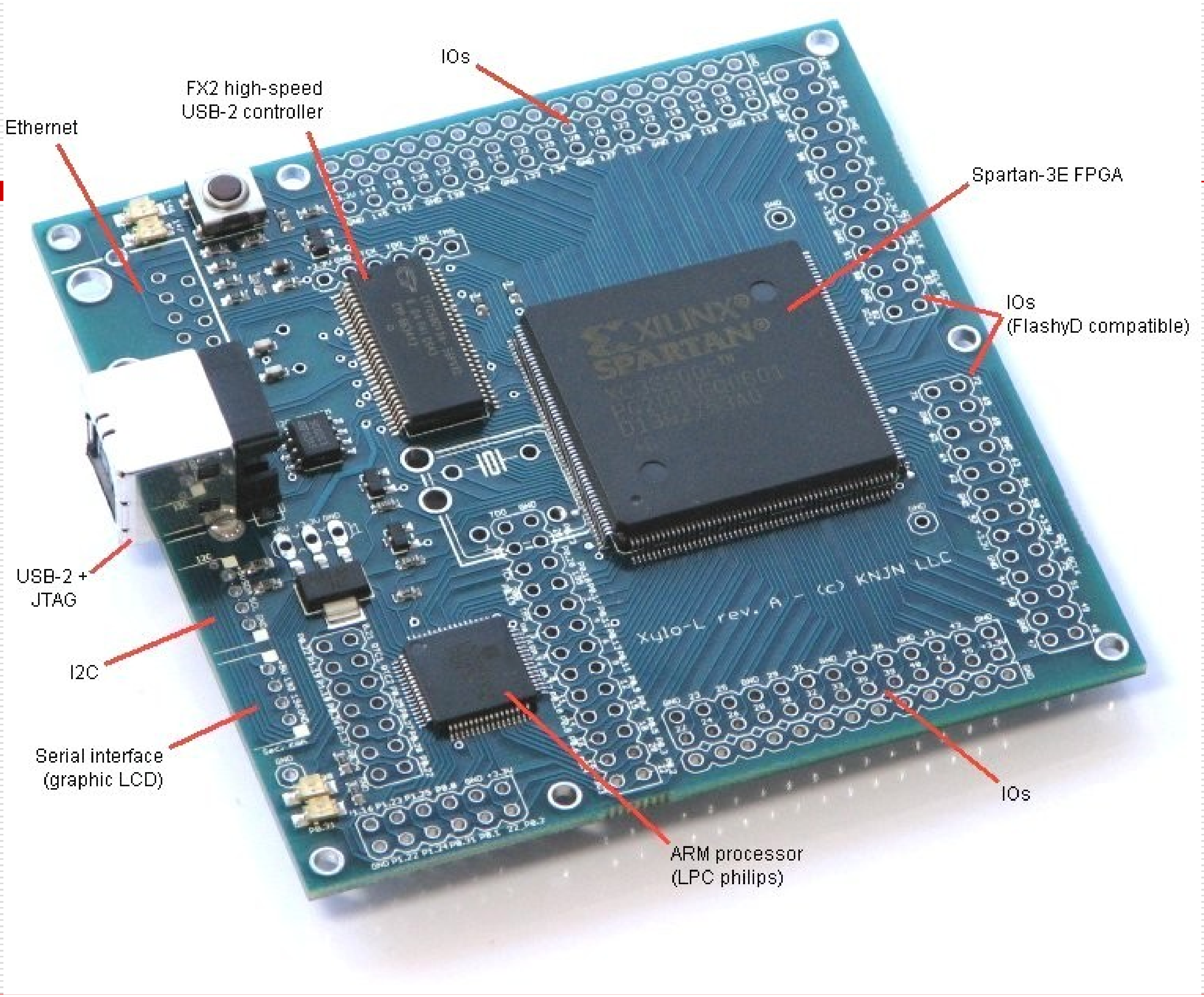


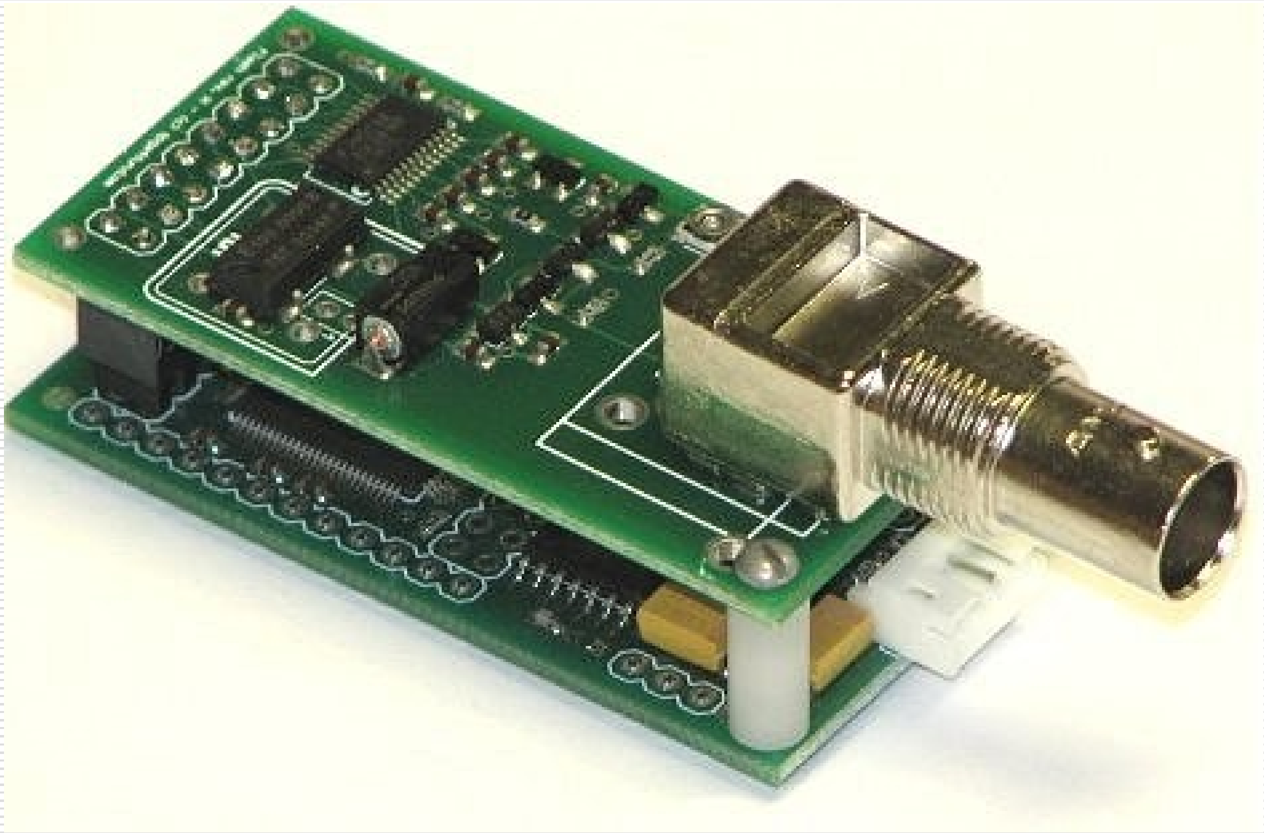
HDL – Verilog

```
module oscillo(clk, RxD, TxD, clk_flash, data_flash);
input clk;
input RxD;
output TxD;

input clk_flash;
input [7:0] data_flash;
wire [7:0] RxD_data;
async_receiver
async_rxd(.clk(clk), .RxD(RxD), .RxD_data_ready(RxD_data_ready), .RxD_data(
RxD_data));

reg startAcquisition;
wire AcquisitionStarted;

always @(posedge clk)
if(~startAcquisition)
  startAcquisition <= RxD_data_ready;
else
if(AcquisitionStarted)
  startAcquisition <= 0;

reg startAcquisition1; always @(posedge clk_flash) startAcquisition1 <=
startAcquisition ;
```

Development & Evaluation

- FPGA + USB interface evaluation boards from www.knjn.com (Saxo, Xilo)
- 8 bit flash ADCs from KNJN
- 4-12 bit flash ADC evaluation boards from Analog Devices (from MARS)


IOs
FX2 high-speed
USB-2 controller
Ethernet
Spartan-3E FPGA
IOs
(FlashyD compatible)
USB-2 +
JTAG
I2C
Serial interface
(graphic LCD)
IOs
ARM processor
(LPC philips)



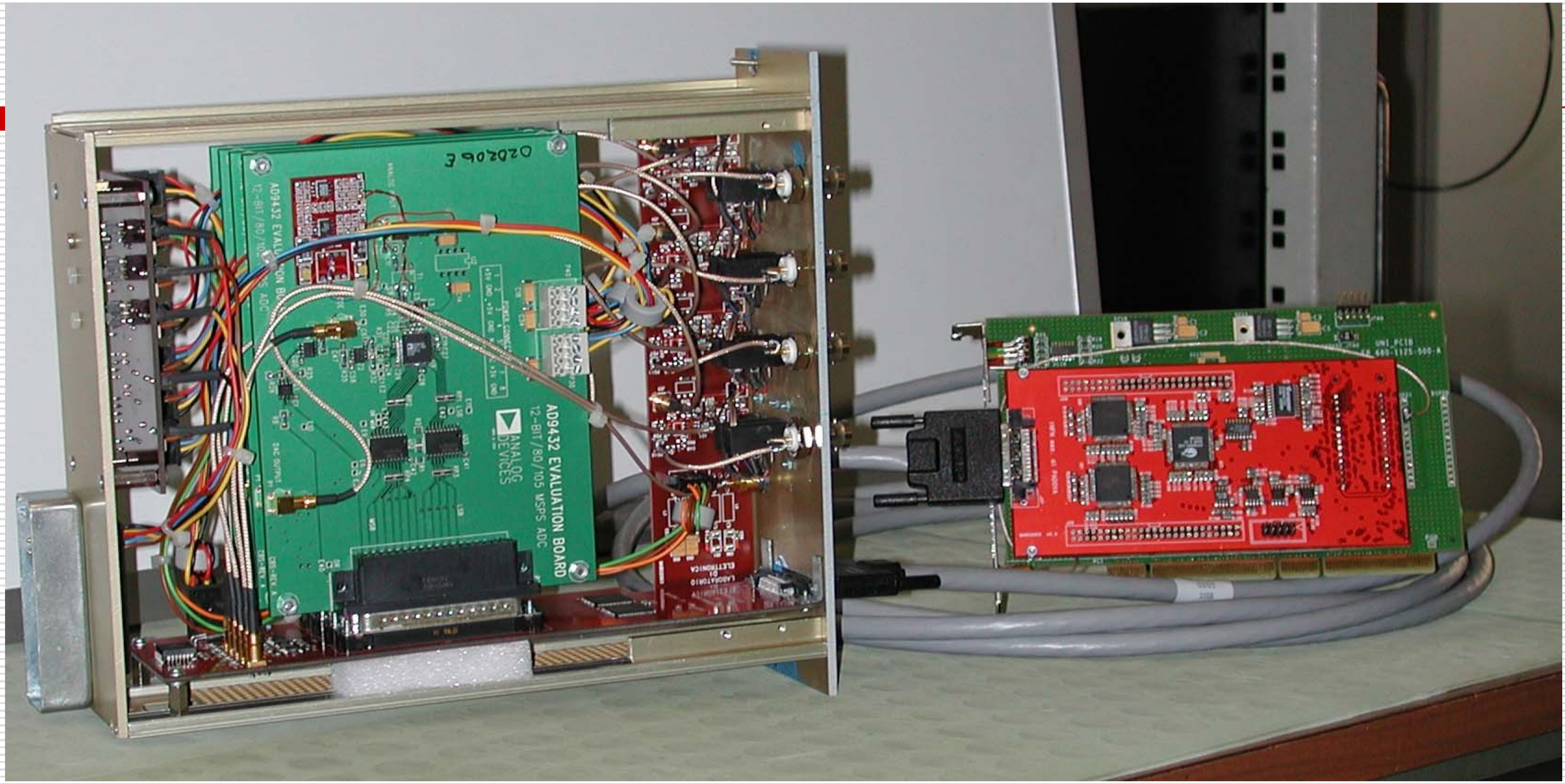
A simple MCA

- Using the evaluation modules we have.
- With 8 bits ADC - not really useful for real measurements
- Simple software developed implements all DPP, histogramming, display and an "oscilloscope" to inspect the signal at various points in the DPP chain.
- May be used in experimental courses at our Institute (e.g. Compton scattering experiment)

What Have to be Done

- Learn better to program in Verilog
- Introduce all DPP in the FPGA
- Develop a trigger system to control 4 12 bits ADCs. This could be a simple system to be used in our lab.
- Develop a board with USB interface, larger FPGA, capable to interface more ADCs.

4 Ge Detectors Digitizing System



1 Double NIM-size module Replacing all electronics (1 full NIM Bin) and DAC System (Camac Crate)

Who are we?

- RVR – DPP algorithms (on the PC) and acquisition software
- Felipe L. Borges (electronic engineering undergraduate student)– FPGA programming

Conclusions

- *DPP will be wide spread in the near future. Costs are much smaller than traditional electronics (~US$500/channel)*
- *Even if commercial systems are now available, they are (now) to much specific. We certainly will need to build our own.*
- *Digital electronics at high frequency is not simple, but way more easy to construct than the analogical equivalents.*

Data Acquisition System SADE – Lab. Pelletron, 1972